Bus based parallel computers: A viable way for massive parallelism

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Abstract. In most distributed memory MIMD multiprocessors, processors are connected by a point-to-point interconnection network. Since interprocessor communication frequently constitutes serious bottlenecks, several architectures were proposed that enhance point-to-point topologies with the help of multiple bus systems so as to improve the communication efficiency. In this paper we study global communication on parallel architectures where the communication means are constituted *solely* by busses. We focus on the *hyperpath* and the *hypergrid* architectures, which are the bus-based versions of the well used point-to-point linear and grid interconnection networks. Using (hyper) graph theoretic concepts in order to model inter-processor communication in such networks, we developed a new tool called *simplification* in order to give extremely efficient algorithms for gossiping (all-to-all or total exchange communications).

1 Introduction

In most distributed memory MIMD multiprocessors, processors are connected by a point-to-point interconnection network. Since interprocessor communication frequently constitutes serious bottlenecks, several architectures were proposed to *enhance* point-to-point topologies with the help of multiple bus systems so as to improve the communication efficiency.

In this paper we study massively parallel systems where processors are connected by using *solely* by busses. These architectures can use the power of bus technologies, providing a way to interconnect much more processors in a simple and efficient manner. This represents a major issue in the construction of parallel computers, because a multiprocessor system with a large number (on the order of thousands) of processors cannot be provided with full connectivity and need

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