On the Circuit Cover Problem for Mixed Graphs*

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Abstract. The circuit cover problem for mixed graphs (those containing edges and/or arcs) is defined as follows. Given a mixed graph M with a nonnegative integer weight function p on its edges and arcs, decide whether (M, p) has a *circuit cover*, that is, a list of circuits in M such that every edge (arc) e is contained in exactly $p(e)$ circuits of the list. In the special case M is a directed graph (contains only arcs) the problem is easy, but when M is an undirected graph not many results are known. For general mixed graphs this problem was shown to be NP-complete by Arkin and Papadimitriou in 1986. We prove that this problem remains NP-complete for *planar* mixed graphs. Furthermore, we present a good characterization for the existence of a circuit cover when M is *series-parallel* (a similar result holds for the fractional version). We also describe a polynomial algorithm to find such a circuit cover, when it exists. This is an ellipsoid-based algorithm whose separation problem is the minimum circuit problem on series-parallel mixed graphs, which we show to be polynomially solvable. Results on two well-known combinatorial problems, the problem of detecting negative circuits and the problem of finding shortest paths, are also presented. We prove that both problems are NP-hard for planar mixed graphs.

Keywords: algorithm, circuit cover, negative circuit, shortest path, mixed graph, series-parallel graph.

1 Introduction

A **mixed graph** is a triplet $M = (V, E, A)$ where V is a finite set of vertices, E is a finite set of edges and A is a finite set of arcs. When $E = \emptyset$ we say that M is a **directed graph**, and when $A = \emptyset$ we say that M is an **undirected graph**. We denote by (M, p) a mixed graph M with a weight function $p : E \cup A \to \mathbb{Q}_+$.

Most of the concepts defined for undirected and directed graphs (see [6]) can be extended in a natural way to mixed graphs. We assume the reader is familiar with them. For a weight function $p : E \cup A \to \mathbb{Q}$ we denote by $p(F)$ the sum $\sum_{e \in F} p(e)$, for any $F \subseteq E \cup A$.

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We use the capital letters D, G and M for directed, undirected and mixed graphs, respectively. In a context referring to a mixed graph M, we may denote by $V(M), E(M)$ and $A(M)$ the set of vertices, edges and arcs of M, respectively.

Here we consider only paths and circuits whose arcs (if any) are oriented in the same direction.

If $M = (V, E, A)$ is a mixed graph and $e \in E \cup A$, then $M - e$ (respectively, M/e) denotes the graph obtained from M by deleting (respectively, contracting) e. A graph H is a **minor** of a graph G (or G has an H-minor) if a graph isomorphic to H can be obtained from a subgraph of G by a sequence of edge contractions. We say that M is **series-parallel** if the underlying graph of M does not have a K_4-minor.

For a mixed graph $M = (V, E, A)$, and a vertex set $X \subseteq V$, we denote by $\delta^+(X)$ (respectively, $\delta^-(X)$) the set of arcs leaving (respectively, entering) X. If $Y \subseteq V$ then the set of edges with an endnode in X and the other in Y is denoted by $\delta(X, Y)$; and if $Y = V - X$ then we write simply $\delta(X)$. The cut defined by X is denoted by $\nabla(X) := \delta(X) \cup \delta^-(X) \cup \delta^+(X)$.

We say that (M, p) has a **circuit cover** if there is a vector of nonnegative integer coefficients $(\lambda_C : C \in \mathcal{C})$, where $\mathcal{C}$ denotes the set of circuits of M, such that $p = \sum_{C \in \mathcal{C}} \lambda_C \chi^C$. Here, for any subgraph H of M, χ^H denotes the {0,1}-incidence vector of the {edge,arc}-set of H. We also say that (M, p) has a **fractional circuit cover** if there is a vector of nonnegative rational coefficients $(\lambda_C : C \in \mathcal{C})$ such that $p = \sum_{C \in \mathcal{C}} \lambda_C \chi^C$.

Given (M, p), where p is a nonnegative integer weight function, the problem of deciding whether (M, p) has a *circuit cover* is called the **Circuit Cover Problem**. The **Fractional Circuit Cover Problem** is defined in a similar way. We are interested in characterizing the existence of solutions for these problems, and in polynomial algorithms to solve them.

For directed graphs the (Fractional) Circuit Cover Problem is easy: *a pair (D, p) has a fractional circuit cover if and only if $p(\delta^-(v)) = p(\delta^+(v))$ for every $v \in V(D)$.* Furthermore, if in addition p is integer-valued then there exists a circuit cover. It is also easy to see that we can find such a cover in polynomial time. This is a special case of a more general result, due to Hoffman [8], related to circulations in directed graphs.

For undirected graphs, the Fractional Circuit Cover Problem was solved by Seymour [13]. He showed that *(G, p) has a fractional circuit cover if, and only if, for every cut $\delta(X)$ we have $p(\delta(X) - e) \geq p(e)$ for each edge e in the cut.* A polynomial algorithm to find such a fractional circuit cover is described in [4].

In the undirected case the fractional version is quite different from the integral version. Clearly, the additional condition "$p(\delta(X))$ is even for every $X \subseteq V(G)$" is necessary for the existence of a circuit cover of (G, p). But it is not always sufficient as shows the following counterexample: let $G = P_{10}$ be the Petersen graph and F a perfect matching of P_{10}; take $p_{10}(e) = 2$ for $e \in F$, and $p_{10}(e) = 1$, otherwise.

Seymour [13] proved that if G is planar then this parity condition together with the above condition (for fractional circuit cover) characterizes the existence of a circuit cover. Alspach, Goddyn and Zhang [1] extended his result showing that, in a certain sense, (P_{10}, p_{10}) is a minimal counterexample. They showed that: *if G has no Petersen graph as a minor, then (G, p) has a circuit cover if, and only if, for every cut $\delta(X)$ we have $p(\delta(X))$ even and $p(\delta(X) - e) \geq p(e)$ for each edge e in the cut.* To our knowledge, their proof does not give (at least immediately) a polynomial algorithm to find a circuit cover (when the conditions are fullfiled). It remains an open problem to find such an algorithm.

Arkin and Papadimitriou [4, 5] have shown that the Circuit Cover Problem and the Fractional Circuit Cover Problem are NP-complete for general mixed graphs. In their paper, they left open the natural question about the complexity of both problems for planar mixed graphs.

We are concerned here with the complexity of the Circuit Cover Problem and the Fractional Circuit Cover Problem for *series-parallel* and *planar* mixed graphs. We show good characterizations and polynomial algorithms for both problems restricted to series-parallel mixed graphs. Furthermore, we settle the question of Arkin and Papadimitriou proving that both problems are NP-complete for planar mixed graphs.

This paper is organized as follows. In Section 2 we show a good characterization for the existence of a (fractional) circuit cover of (M, p) when M is a series-parallel mixed graph. Section 3 is devoted to the description of a polynomial algorithm (relying on the ellipsoid method) that finds a circuit cover of (M, p) (if it exists), when M is series-parallel. In Section 4 we describe a polynomial algorithm to find a minimum circuit in a series-parallel mixed graph with arbitrary weights. Finally, in Section 5 we prove that the Circuit Cover Problem and the Fractional Circuit Cover Problem are NP-complete for planar mixed graphs.

A preliminary version of this paper, without some of the proofs and the results of Section 5, has appeared in [11].

2 Circuit covers in series-parallel mixed graphs

We turn now to the study of the (Fractional) Circuit Cover Problem for mixed graphs. In 1986 Arkin and Papadimitriou [4] showed that the Circuit Cover Problem for mixed graphs is NP-complete. In view of this result, it is unlikely that we can find nice necessary and sufficient conditions for the existence of a circuit cover in an arbitrary mixed graph (M, p). We show that for series-parallel mixed graphs such a nice characterization exists.

The following conditions are clearly necessary for the existence of a fractional circuit cover of (M,p):

(a) For every $X \subseteq V$, $f_p(X) := p(\delta(X)) - |p(\delta^-(X)) - p(\delta^+(X))| \geq 0$;

(b) For every cut $\nabla(X)$ and every $e \in \delta(X)$, $p(\nabla(X) - e) \geq p(e)$.

Furthermore, if (M,p) has a circuit cover then it is necessary that p is nonnegative integral and the following holds:

(c) For every cut $\nabla(X)$, $p(\nabla(X))$ is even.

We say that (M,p) is **balanced** if it satisfies (b); **eulerian** if it satisfies conditions (a) and (c); and **fractionally admissible** if it satisfies (a) and (b). If p is integral, we say that (M,p) is **admissible** if it is eulerian and balanced (or, it is fractionally admissible and satisfies (c)). Sometimes, we say simply that p is balanced, eulerian or (fractionally) admissible.

The following example shows that (fractional) admissibility is not always a sufficient condition for the existence of a (fractional) circuit cover. Take the mixed graph K_4' whose underlying graph is isomorphic to K_4, and whose directed part consists of a directed circuit of length 4 and the undirected part consists of a 1-factor. Assign weight 1 to the arcs and weight 2 to the edges of K_4'. It easy to see that K_4' with these weights is (fractionally) admissible and does not have a (fractional) circuit cover.

The main result of this section is the proof that admissibility is a sufficient condition for the existence of a circuit cover when M is series-parallel. We need two lemmas. The proof of the first one is not difficult and is left to the reader.

Lemma 2.1. *Let G be a series-parallel undirected graph, B a minimal cut of G and C a circuit of G. Then $|B \cap C| \leq 2$.* ■

Lemma 2.2. *Let (M,p) be an admissible pair. Consider a subset $X \subset V(M)$ and an edge $e = uv \in \delta(X)$, $u \in X$, such that $p(e) > 0$, $f_p(X) = 0$ and $p(\delta^-(X)) - p(\delta^+(X)) > 0$. Let M' be the graph obtained from M by replacing e with an arc $a = (u,v)$; and let p' be the weight function on M', obtained from p by setting $p'(a) := p(e)$. Then, the resulting pair (M',p') is admissible.*

Proof. First we prove the lemma for the case $p(e) = 1$. In this case, suppose by contradiction that (M',p') is not admissible. Clearly, conditions (b) and (c) are satisfied by (M',p'); thus, we conclude there exists some subset $Y \subseteq V(M)$ such that $e \in \delta(Y)$ and $f_{p'}(Y) < 0$. We can assume that $v \in Y$.

For ease of notation we set $h(S) := p(\delta^-(S)) - p(\delta^+(S))$ for any subset S of $V(M)$. In what follows h refers only to the pair (M,p). Since $f_{p'}(Y) = p(\delta(Y) - e) - |h(Y) + 1|$, and $f_{p'}(Y) < 0$, we have

$$p(\delta(Y) - e) < |h(Y) + 1|. \tag{1}$$

First, suppose $h(Y) < 0$. In this case, $|h(Y)+1| = |h(Y)| - 1$. Thus, using inequality (1) we conclude that $p(\delta(Y)) - 1 < |h(Y)| - 1$, and therefore $f_p(Y) = p(\delta(Y)) - |h(Y)| < 0$, a contradiction to the admissibility of (M,p).

Hence, $h(Y) \geq 0$. In this case, since $p(e) = 1$, inequality (1) simplifies to $p(\delta(Y)) < h(Y) + 2$.

By our assumption, $f_p(X) = 0$ and $h(X) > 0$. Thus, $p(\delta(X)) = h(X)$. Combining this equality with the last inequality for $p(\delta(Y))$ we have

$$p(\delta(X)) + p(\delta(Y)) < h(X) + h(Y) + 2.$$

Since h is a modular function, that is, $h(X)+h(Y) = h(X \cap Y) + h(X \cup Y)$, we obtain

$$p(\delta(X)) + p(\delta(Y)) < h(X \cap Y) + h(X \cup Y) + 2.$$

Now since

$$\begin{aligned} p(\delta(X)) + p(\delta(Y)) &= p(\delta(X \cap Y)) + p(\delta(X \cup Y)) + 2p(\delta(X - Y, Y - X)), \\ h(X \cap Y) &\leq |h(X \cap Y)| = p(\delta(X \cap Y)) - f_p(X \cap Y), \\ h(X \cup Y) &\leq |h(X \cup Y)| = p(\delta(X \cup Y)) - f_p(X \cup Y), \end{aligned}$$

substituting them in the above inequality, we obtain the following contradiction:

$$2 = 2p(e) \leq 2p(\delta(X - Y, Y - X)) < -f_p(X \cap Y) - f_p(X \cup Y) + 2 \leq 2.$$

This shows that (M', p') is admissible when $p(e) = 1$.

If $p(e) \geq 2$ we replace the edge e with $p(e)$ parallel edges, and assign weight 1 to each of them. Clearly, the resulting weighted mixed graph (M'', p'') is admissible. Using the lemma in the case of unit weight (which we just proved) for (M'', p''), we conclude that we can replace each parallel edge uv with an arc (u, v) and the new pair (M', p') is still admissible. Finally, replacing the $p(e)$ parallel arcs (u, v) with an arc (u, v) of weight $p(e)$, we still preserve admissibility. This concludes the proof.

■

The proof of the main theorem was inspired by the proof given by Seymour [13] for undirected planar graphs, and by the proof of the theorem of Alspach *et al.* [1] mentioned before.

Theorem 2.1. *If M is series-parallel then (M,p) has a circuit cover if and only if p is admissible.*

Proof. It is immediate that if (M,p) has a circuit cover then p is admissible. To prove the converse, let us assume that (M,p) is an admissible pair and $p(e) > 0$ for every

$e \in E \cup A$ (otherwise we could delete e from M). Applying Lemma 2.2 we can also assume that if $f_p(X) = 0$ then $\delta(X) = \emptyset$.

We use induction on $p(E)$. If $p(E) = 0$ then M is a directed graph and $p(\delta^-(v)) = p(\delta^+(v))$ for every $v \in V(M)$. The result is immediate.

Suppose that $p(E) > 0$. If there is a cut $\nabla(X)$ such that $|\nabla(X)| = |\delta(X)| = 2$, then we can contract one of the edges of this cut and apply the induction hypothesis. Thus, we can assume that there are no such cuts.

If there is an edge e_0 with $p(e_0) = 1$ then we can assign an arbitrary orientation to e_0. Since $f_p(X) \geq 2$ for every $\emptyset \neq X \subset V$ such that $e_0 \in \delta(X)$, it follows that the resulting pair (M', p') is admissible. Using the induction hypothesis the result follows.

Let e_0 be an edge such that $p(e_0)$ is maximum. We can suppose that $p(e_0) \geq 2$. Let $p' = p - 2\chi^{e_0}$. We claim that (M, p') is admissible. Clearly, (M, p') is eulerian. It remains to show that (M, p') is balanced. Suppose by contradiction that there is a cut $\nabla(X)$ such that $p'(\nabla(X) - e) < p'(e)$ for some edge $e \in \delta(X)$. Clearly, $e_0 \in \delta(X)$. If $e = e_0$ then

$$p(\nabla(X) - e_0) = p'(\nabla(X) - e_0) < p'(e_0) < p(e_0),$$

which contradicts the admissibility of (M, p). Hence, $e \neq e_0$. Since $p'(\nabla(X))$ is even, we have $p'(\nabla(X) - e) \leq p'(e) - 2$. On the other hand,

$$p(e_0) \leq p(\nabla(X) - e) = p'(\nabla(X) - e) + 2 \leq p'(e) = p(e).$$

But then $p(e_0) = p(e)$ and $|\nabla(X)| = |\delta(X)| = 2$, contradicting the nonexistence of such cuts.

Thus (M, p') is admissible and $p'(E) = p(E) - 2$. By the induction hypothesis, (M, p') has a circuit cover. Then there is a list L (with possible repetitions) of circuits such that $p' = \sum_{C \in L} \chi^C$. Let $L = L_0 \cup L_1$, where the circuits in L_0 contain $e_0 = xy$ and the circuits in L_1 do not contain e_0.

Define an auxiliary undirected graph H as follows. Take $V(H) := V$ and for each $C \in L_1$ construct in H a circuit C that is the underlying circuit of C. Label the edges of this circuit with "C". We claim that there is a path from x to y in H.

In fact, let X be the set of vertices that are reachable from x in H, and suppose $y \notin X$. Let B be a minimal cut of M contained in $\nabla(X)$ such that $e_0 \in B$. Then no circuit of L_1 uses an edge or an arc of B, and by Lemma 2.1, every circuit of L_0 uses e_0 and only one element of B different from e_0. Thus $p(B - e_0) = p'(B - e_0) = p'(e_0) = p(e_0) - 2$, which contradicts the admissibility of (M, p). Therefore, $y \in X$.

Take a shortest path from x to y in H. For each section of this path corresponding to edges with the same label, take only one representative, and consider the sequence of such labels, say $(C_1, \ldots, C_k)$. Clearly, there are no repeated circuits and $V(C_i) \cap V(C_j) \neq \emptyset$ if and only if $|i - j| = 1$.

Consider the subgraph G of H induced by the edge e_0 together with the edges in the circuits $C_1, \ldots, C_k$. We claim that $|V(C_i) \cap V(C_{i+1})| = 1$ for $i = 1, \ldots, k-1$. Suppose by contradiction that there are circuits $C = C_i$ and $C' = C_{i+1}$ such that $|V(C) \cap V(C')| \geq 2$. In this case, it is not difficult to prove that we can find two distinct vertices $a, b \in V(C) \cap V(C')$ and two other distinct vertices $u \in V(C) - V(C')$ and $v \in V(C') - V(C)$, and also a path P_{xu} from x to u in G and a path P_{yv} from y to a vertex v such that $P_{xu} \cup C \cup C' \cup P_{yv} \cup \{e_0\}$ contains a subgraph homeomorphic to K_4 (note the roles of the vertices a, b, u, v in this homeomorphism). This is a contradiction since M is series-parallel.

Thus $|V(C_i) \cap V(C_{i+1})| = 1$, for $i = 1, \ldots, k-1$. It is easy to see that $\bigcup C_i$ can be partitioned into a path from x to y and a path from y to x, say, P' and Q'. Each one of these paths together with the edge e_0 forms a circuit in M. Let P, Q be these two circuits. Consider now the list of circuits $L' := L - \{C_1, \ldots, C_k\} \cup \{P, Q\}$. By construction, L' contains only circuits of M, and furthermore $p = \sum_{C \in L'} \chi^C$. This shows that (M, p) has a circuit cover. ■

The above theorem gives immediately a result for the Fractional Circuit Cover Problem.

Corollary 2.1. *If M is series-parallel then (M, p) has a fractional circuit cover if and only if p is fractionally admissible.* ■

To conclude this section we note that the property of being admissible is checkable in polynomial time. To check condition (c) we only have to verify whether $p(\nabla(v))$ is even for every $v \in V$. To check condition (b) we can do the following. Let H be the underlying graph of M. For each edge $e = uv$ in M compute a minimum weight cut B_e, separating u from v, with respect to p in $H - e$. If for some pair (e, B_e) we have $p(B_e) < p(e)$, then condition (b) is not satisfied, otherwise it is. Finally, we can check condition (a) in the following way. First note that (a) holds if and only if $q(X) := p(\delta(X)) - p(\delta^-(X)) + p(\delta^+(X)) \geq 0$ for every $X \subseteq V$. Let $D = (V, A \cup A')$ be the directed graph obtained from M by replacing each edge with two arcs defining a circuit. Set capacities $l(a) = u(a) = p(a)$ for $a \in A$ and $l(a') = 0, u(a') = p(e)$ for each $a' \in A'$ belonging to the circuit that replaced e. It is clear now that condition (a) is satisfied if and only if D, l, u satisfy Hoffman's condition (see [2]). This can be checked by a single max-flow computation (see [2], Sec. 6.7).

3 A polynomial algorithm to find a circuit cover in a series-parallel mixed graph

Let be given an admissible pair (M, p), where $M = (E, A, V)$ is series-parallel. A circuit cover of (M, p) can be represented by a pair (L, μ), where L is a list (without repetitions) of circuits of M and μ is a vector indicating the multiplicity of each circuit. It is not clear whether there exists such a list L with a polynomially bounded number of circuits. Our proof of Theorem 2.1 does not answer this question. However, we can prove that there exists such a list with at most $m := |E \cup A|$ circuits [12]. In polyhedral terminology, this is equivalent to saying that if p is in the integer cone generated by the (incidence vectors of) circuits of M (p is admissible) then p can be expressed as a nonnegative integer linear combination of at most m circuits of M.

Unfortunately, our proof of the latter result does not give directly a polynomial algorithm to find such a circuit cover. However, if we do not require that the circuit cover uses at most m circuits then we can design a polynomial algorithm that relies on the ellipsoid method. For that, we need a polynomial separation algorithm that is interesting in its own right: finding a minimum circuit in a series-parallel mixed graph with arbitrary weights.

We describe two algorithms to find a circuit cover. The first algorithm is based on the proof of Theorem 2.1 but it has a pseudo-polynomial running time. The second algorithm is an elegant polynomial procedure that uses the first one and is based on the algorithm presented in [1].

CirCov1 Algorithm

Input: An admissible pair (M, p), where $M = (V, E, A)$ is series-parallel.
Output: A circuit cover L' of (M, p).

1. Delete arcs and edges with weight 0. Contract any edge that is in a cut $\nabla(X)$ such that $|\nabla(X)| = |\delta(X)| = 2$. If there is an edge e in a cut $\nabla(X)$ such that $f_p(X) = 0$ then assign an orientation to e according to Lemma 2.2.

2. If $p(E) = 0$ then return a circuit cover L' (for directed graphs this is trivial) and halt.

3. If there is an edge with weight 1 then assign an arbitrary orientation to it. Call CirCov1 recursively to find a circuit cover L' of the new graph, return L' and halt.

4. Let $e_0 = xy$ be an edge with maximum weight. Call CirCov1 recursively to find a circuit cover L' of $(M, p - 2\chi^{e_0})$.

5. As in the proof of Theorem 2.1, find a shortest (x, y)-path in the auxiliary undirected graph H. Let $\{C_1, \ldots, C_k\}$ be the arc labels along this path. Decompose $\bigcup C_i$ into an (x, y)-path P' and a (y, x)-path Q'. Let $P := P'(y, e_0, x)$ and $Q := Q'(x, e_0, y)$.
   Return the circuit cover $L := L - \{C_1, \ldots, C_k\} \cup \{P, Q\}$ and halt.

Step 1 requires $O(|E|)$ max-flow min-cut computations. Step 2 can be done in $O(|A| \cdot |V|)$ time. The total number of calls of CirCov1 is bounded by $p(E)/2$ as the total weight of the edges in each successive pair (M, p) is reduced by 2. So CirCov1 is a pseudo-polynomial algorithm.

We discuss now how to obtain a polynomial algorithm from CirCov1. The idea is to formulate the Circuit Cover Problem for (M, p) as an integer program and to solve its relaxation (that is, we solve the Fractional Circuit Cover Problem for (M, p)). Then we use the fractional part of the resulting solution to define a new weight p' (with relatively small entries), and call CirCov1 to solve the Circuit Cover Problem for (M, p'). A circuit cover of (M, p) is obtained by adjoining the partial circuit cover corresponding to the integral part of the linear program solution and the circuit cover found by CirCov1.

In what follows, N denotes the circuit-{edge,arc} incidence matrix of M and $\mathbf{1}$ denotes the vector of $|\mathcal{C}|$ ones.

CirCov2 Algorithm

Input: An admissible pair (M, p), where $M = (V, E, A)$ is series-parallel.

Output: A circuit cover (L, μ) of (M, p), where L is a list containing at most $2|E \cup A| - 1$ circuits and μ is a multiplicity vector whose entries are bounded by $r := \max\{p(e) : e \in E \cup A\}$.

1. Find a basic feasible solution $\lambda = (\lambda_C)_{C \in \mathcal{C}}$ of the following linear program:
$$\max\{\lambda \mathbf{1} : \lambda N = p,\ \lambda \geq 0\}. \tag{2}$$
2. Let $\lfloor \lambda \rfloor := (\lfloor \lambda_C \rfloor)_{C \in \mathcal{C}}$ and $\{\lambda\} := \lambda - \lfloor \lambda \rfloor$ be respectively the integral and the fractional part of λ, and let $p' := \{\lambda\} N = p - \lfloor \lambda \rfloor N$. (Note that, since p' is a nonnegative combination of circuits, (M, p') is fractionally admissible. As p and $\lfloor \lambda \rfloor N$ are eulerian, then p' is also eulerian.)
3. Call CirCov1 with input (M, p') to obtain a circuit cover L' of (M, p').
4. Adjoin L' to the circuit cover $(S, \lfloor \lambda \rfloor)$, where $S := \{C \in \mathcal{C} : \lfloor \lambda_C \rfloor > 0\}$, and return the resulting circuit cover (L, μ). Halt.

Let us show that $|L|$ is polynomially bounded. As λ is a basic solution, we have $|S| \leq |E \cup A|$. Furthermore, $|L'| + \lfloor \lambda \rfloor \mathbf{1} \leq \lambda \mathbf{1} = \lfloor \lambda \rfloor \mathbf{1} + \{\lambda\} \mathbf{1}$, and so $|L'| \leq \{\lambda\} \mathbf{1}$. Since each nonzero entry in $\{\lambda\}$ is less than 1 we have $\{\lambda\} \mathbf{1} < |E \cup A|$ and therefore $|L'| \leq |E \cup A| - 1$. Thus $|L| \leq |S| + |L'| \leq 2|E \cup A| - 1$. As $\max\{p'(e) : e \in E \cup A\} \leq |L'| < |E \cup A|$, we conclude that Step 3 can be done in polynomial time.

It remains to show how to solve Step 1 in polynomial time in $|E \cup A| \log(r)$, despite the exponential number of variables λ_C. For that, consider the dual linear program of (2): $\min\{px : Nx \geq \mathbf{1}\}$. The *separation problem* for this LP is the following: *Given a rational vector x, either certify that x satisfies $Nx \geq \mathbf{1}$, or find a violated inequality (a circuit in (M, x) having weight less than 1).*

A theorem of Grötschel, Lovász and Schrijver (see [7]) implies that a basic optimal solution of (2) can be found via the ellipsoid method in time polynomially bounded by $|E \cup A|$ and the input length of p, provided that we can solve the above separation problem in time polynomially bounded by $|E \cup A|$ and the input length of x. For that, we can use a polynomial algorithm that finds a minimum circuit in the weighted series-parallel mixed graph (M, x). In the next section we provide such an algorithm.

Theorem 3.1. *The Circuit Cover Problem and the Fractional Circuit Cover Problem for series-parallel mixed graphs can be solved in polynomial time.* ■

4 Minimum circuits in series-parallel mixed graphs

Consider a series-parallel mixed graph (M, w), where w is an arbitrary weight function. As we are interested in finding minimum circuits, we may assume that M is strongly connected, has at least one circuit and does not have cut vertices. We note that as w can have negative entries, we must deal with negative circuits. We recall that for arbitrary mixed graphs the problem of detecting negative circuits is NP-complete [5].

Clearly, we can compute in polynomial time a minimum circuit of length 2 in M. Thus, it suffices to describe a polynomial algorithm to find a minimum circuit of length at least 3 in M. To solve the latter problem we can restrict ourselves to directed graphs: we replace each edge e of M with two arcs defining a circuit, each one with weight $w(e)$. Thus, it remains to show a polynomial algorithm for the following problem:

MC3P(D,w): Given a series-parallel directed graph (D, w), find, if it exists, a minimum directed circuit C of length at least 3.

The algorithm is based on the existence of a vertex with exactly 2 neighbours. We call such a vertex **special**. A result (easy to be proved) that we use in the sequel is the following.

Lemma 4.1. *If G is a 2-connected series-parallel graph with $|V(G)| \geq 3$ then G has a vertex with exactly two neighbours.* ■

In the description of the algorithm we use following two operations on a directed graph (D, w).

Parallel Arc Deletion - PAD(D, w)

> Consider any two parallel arcs a and b.
> Set $D' := D - b$ and $w(a) := \min\{w(a), w(b)\}$.
> Let w' be the restriction of w to D'.
> Return (D', w').

Special Vertex Elimination - SVE$(D, w; v)$ (D does not have parallel arcs)

Let x and y be the neighbours of the special vertex v.

1. If $(x, v), (v, x), (y, v), (v, y) \in A(D)$ then
   set $D' := D/\{(y, v), (v, y)\}$;
   $w(x, v) := w(x, v) + w(v, y)$; $w(v, x) := w(v, x) + w(y, v)$;
2. If $(x, v), (v, x), (v, y) \in A(D)$ and $(y, v) \notin A(D)$ then
   set $D' := (D - (v, x))/(v, y)$; $w(x, v) := w(x, v) + w(v, y)$;
3. If $(x, v), (v, y) \in A(D)$ and $(v, x), (y, v) \notin A(D)$ then
   set $D' := D/(v, y)$; $w(x, v) := w(x, v) + w(v, y)$;
4. Similarly, deal with the symmetric cases of 2 and 3, with the role of x and y exchanged.

Let w' be the restriction of w to D'.
Return (D', w').

Denote by $\gamma(D, w)$ the weight of a minimum circuit of length at least 3 in (D, w). Clearly, if (D', w') is obtained from (D, w) by a PAD operation then $\gamma(D, w) = \gamma(D', w')$. On the other hand, if (D', w') comes from a SVE operation then $\gamma(D, w) = \min\{w(C), \gamma(D', w')\}$ where C is a minimum circuit of length 3 containing v, x and y (if there is no such a circuit, set $w(C) = +\infty$).

As D is series-parallel and does not have cut vertices it has a special vertex by Lemma 4.1. Moreover, operations PAD and SVE preserve series-parallelness and does not create cut vertices. So, a simple polynomial algorithm that solves MC3P(D, w) consists of successive applications of these two operations, as shown in the following sketch.

MC3 Algorithm
Input: A weighted series-parallel directed graph (D, w).
Output: A minimum circuit in (D, w) of length at least 3.
Set $C := \emptyset$ and set $w(C) := +\infty$;

While $|V(D)| \geq 3$ do
  While (D,w) has parallel arcs do $(D,w) := \mathrm{PAD}(D,w)$;
  If (D,w) has a special vertex v then
    Let C' be a minimum circuit of length 3 containing v;
    (if it does not exist, set $w(C') = +\infty$)
    $(D,w) := \mathrm{SVE}(D,w;v)$;
    If $w(C') < w(C)$ then $C := C'$;
Return the circuit corresponding to C in the original digraph (D,w).

5 Complexity of the Planar Circuit Cover Problem

To show that the Circuit Cover Problem for planar mixed graphs is NP-complete we shall use a special case of 3-SAT, namely, the Planar 3-SAT [10]. An instance of 3-SAT consists of a boolean formula $F(C,X)$ with clauses $C = \{C_1,\ldots,C_m\}$ and variables $X = \{v_1,\ldots,v_n\}$. To define the Planar 3-SAT consider the undirected graph $G(F) := (C \cup X, E_1 \cup E_2)$ where

$$\begin{aligned} E_1 &= \{C_i v_j \ : \ v_j \in C_i \text{ or } \overline{v}_j \in C_i, 1 \leq i \leq m, 1 \leq j \leq n\} \text{ and} \\ E_2 &= \{v_j v_{j+1} \ : \ 1 \leq j < n\} \cup \{v_n v_1\}. \end{aligned}$$

Note that the structure of $G(F)$ depends on the ordering of the variables. Planar 3-SAT corresponds to 3-SAT restricted to formulae $F(C,X)$ for which there exists an ordering of the variables such that $G(F)$ is planar.

Let us describe the reduction from Planar 3-SAT to the planar Circuit Cover Problem. The proof is inspired by a proof of NP-completeness of the Directed Hamiltonian Circuit for planar directed graphs [10].

Suppose that $F(C,X)$ is an instance of Planar 3-SAT and fix an embedding of $G(F)$ in the plane. We can assume that each clause in F contains at least two literals. In Figure 1(i) we have an example of a planar graph $G(F)$.

Consider the directed graph $\vec{G}(F)$ obtained from $G(F)$ as follows. We assign an orientation for the edges in E_2 to obtain a circuit $\vec{C} := (v_1, v_2, \ldots, v_n, v_1)$; then we replace each edge $v_j C_i$ with a directed circuit of length 2. The orientation of each circuit in the plane depends on its position with respect to the directed circuit $\vec{C}$ (oriented in the clockwise direction). If the vertex C_i is in the external region with respect to $\vec{C}$, then it is oriented in the clockwise direction, otherwise it is oriented in the counter-clockwise direction (see Figure 1(ii)).

We construct from $\vec{G}(F)$ a mixed graph (M,p) replacing the vertices of $\vec{G}(F)$ (variables and clauses) with some *super-vertices* (graphs) that we describe in what follows. In this new graph each edge has weight 2 and each arc has weight 1.

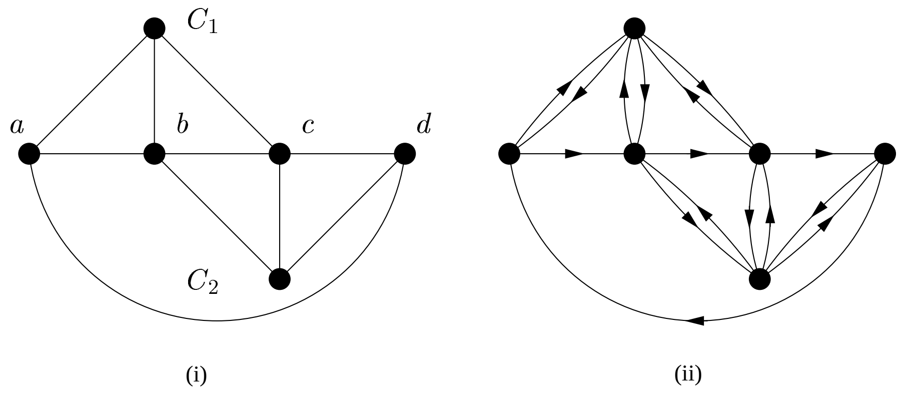

Figure 1: (i) A graph $G(F)$ for the formula $F = (a + \overline{b} + c)(b + c + \overline{d})$. (ii) Graph $\vec{G}(F)$.

We replace each variable v_j with a graph $L(v_j)$ as indicated in Figure 2, identifying each arc (v_j, v_{j+1}) of $\vec{G}(F)$ with an arc (t_j, s_{j+1}), $j = 1, \ldots, n$, where $v_{n+1} = v_1$ and $s_{n+1} = s_1$.

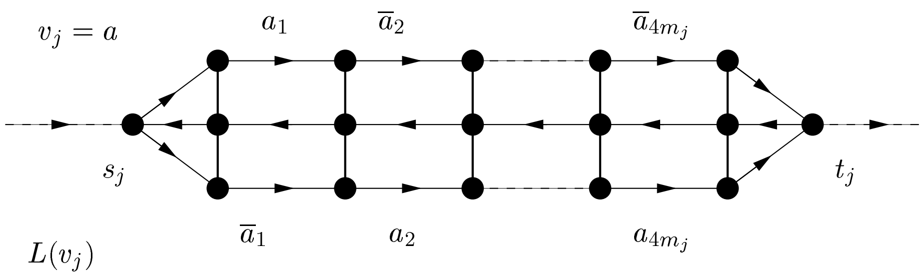

Figure 2: Graph $L(v_j)$ corresponding to the variable v_j.

In the graph $L(v_j)$, m_j is the number of occurrences of the variable v_j (negated or not) in the formula F. The number $4m_j$ is sufficiently large to allow gaps between vertical sections of $L(v_j)$ connecting distinct clauses. The necessity of that will become clear later.

We describe now the super-vertices corresponding to the clauses of F. Suppose that C_i is a clause with three literals. We replace C_i with a graph $H(C_i)$ as indicated in Figure 3(i), where the vertices h_1, h_2, h_3 are identified with the variables of the clause C_i. Note that there is a symmetry between h_2 and h_3 with respect to the structure of (C_i), but h_1 is a distinguished vertex. We say that the edge e_t is the *opposite edge* of h_t, for $t = 2, 3$, and h_1 is the *free vertex* of $H(C_i)$. If C_i is a clause with only two literals then we replace C_i with a graph $H(C_i)$ as indicated in Figure 3(ii). Note that

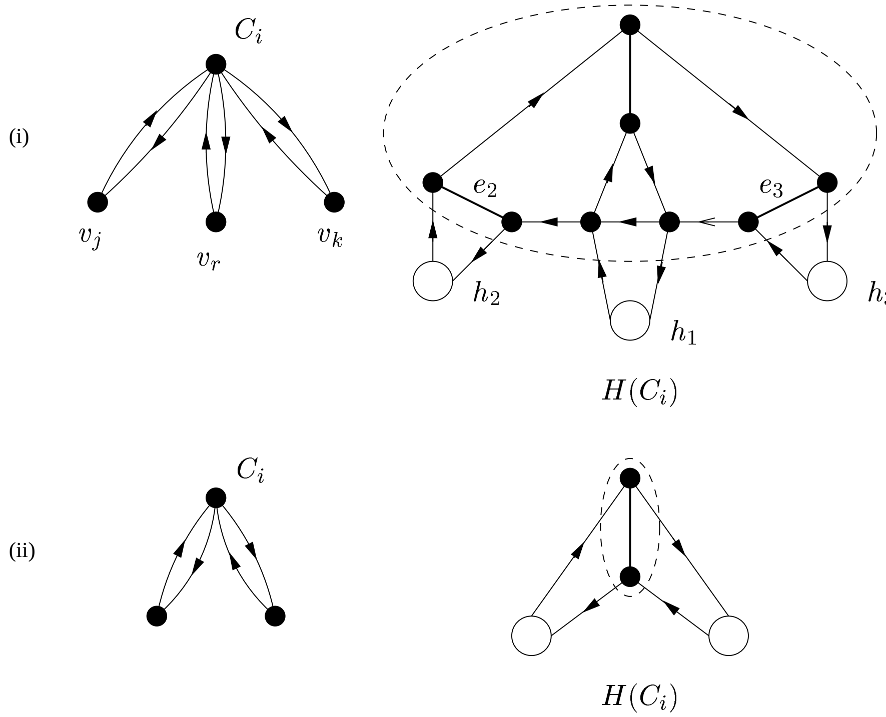

Figure 3: (i) A clause C_i with 3 literals and its corresponding graph $H(C_i)$. (ii) A clause C_i with 2 literals and its corresponding graph $H(C_i)$.

the arcs incident to the vertices h_t represent the arcs incident to the variables of C_i in the graph $\vec{G}(F)$ (see Figure 1(ii)).

Now we show how to connect the clauses with the variables. Let C_i be a clause containing a literal v_j. We connect $H(C_i)$ with $L(v_j)$ as follows. Suppose that v_j is identified with the super-vertex h_t (which corresponds to the graph $L(v_j)$). Remove an arc $a_k = (x, y)$ in $L(v_j)$, identify y with the head of the arc leaving h_t and identify x with the tail of the arc entering h_t. The choice of a_k is arbitrary but there must be gaps between links of distinct $H(C_i)$'s and the replacement should preserve the planarity of the resulting graph. It is not hard to see that this is possible. If C_i contains a literal $\overline{a}_j$, remove an arc $\overline{a}_k = (x, y)$ and connect x, y with $H(C_i)$ as we have done before.

This concludes the construction of the plane mixed graph (M, p). See an example in Figure 4. In this example we used $2m_j$ as the length of each $L(v_j)$ instead of $4m_j$.

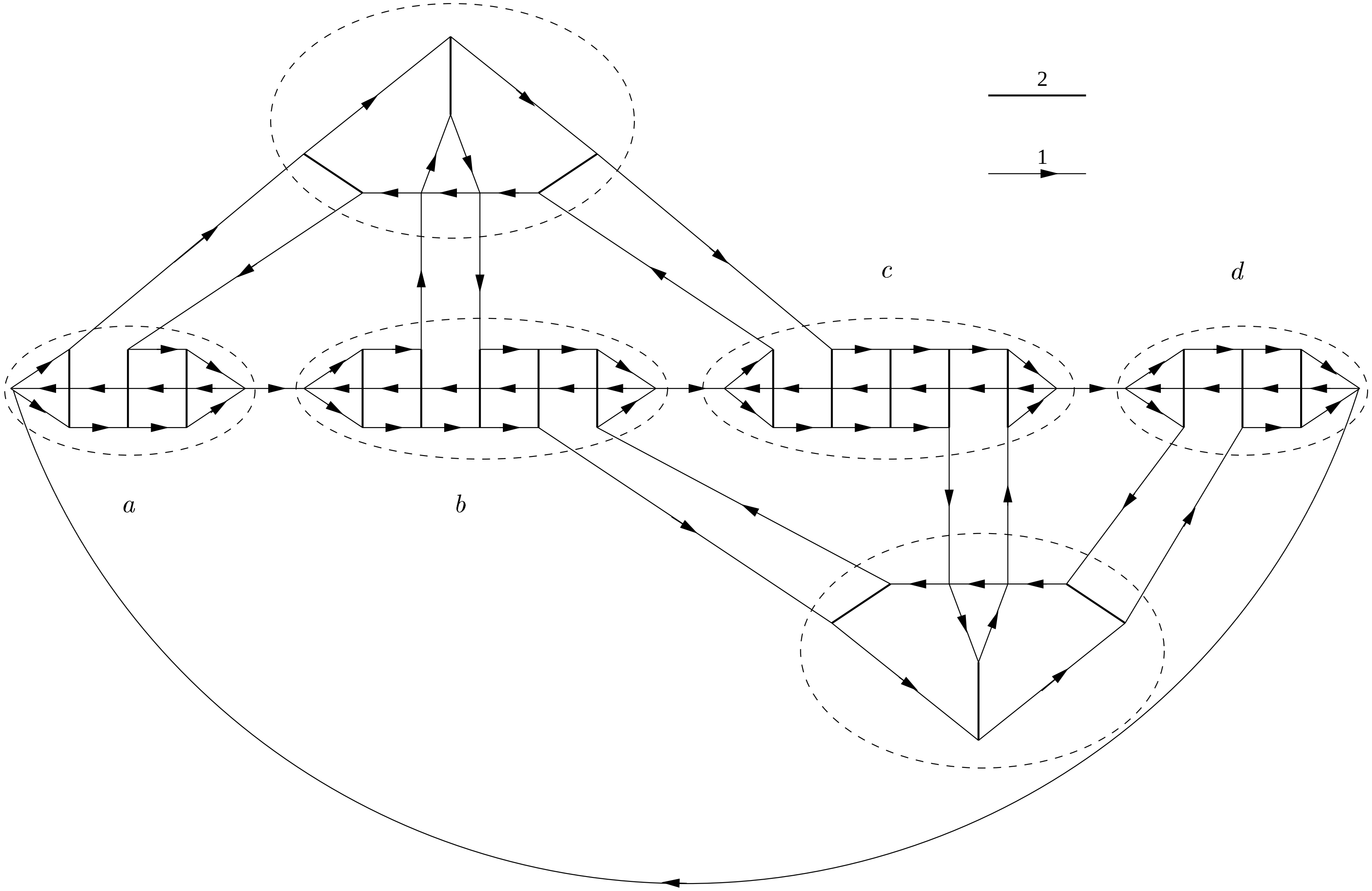

Figure 4: Graph (M, p) obtained from formula $F = (a + \overline{b} + c)(b + c + \overline{d})$.

We show that if (M, p) admits a circuit cover then there exists a circuit (with some special features) which contains every arc (t_j, s_{j+1}), $j = 1, \ldots, n$. First, we make some remarks about the graphs $L(v_j)$ and $H(C_i)$.

The graph $L(v_j)$ with an additional arc (t_j, s_j) admits a circuit cover. There exist two possibilities for the circuit C containing (t_j, s_j): either $C - (t_j, s_j)$ is a path in zigzag that goes from s_j to t_j and contains every arc a_k, for $k = 1, \ldots, 4m_j$ (see Figure 5), or $C - (t_j, s_j)$ is a path in zigzag that goes from s_j to t_j and contains every arc $\overline{a}_k$, for $k = 1, \ldots, 4m_j$. The other arcs and edges can be covered by local circuits.

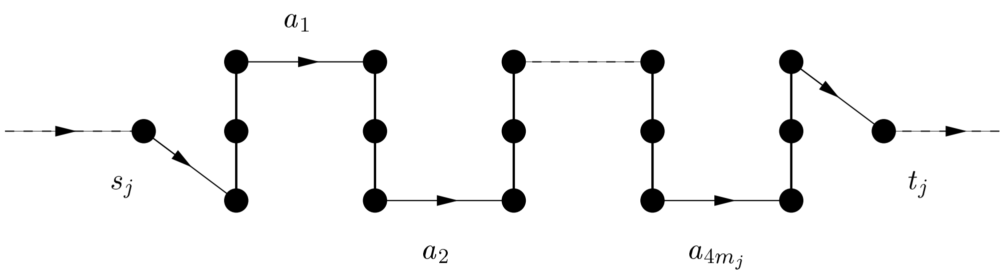

Figure 5: Zigzag path.

The graph $H(C_i)$ (thinking of h_t as a vertex) admits a circuit cover. This cover is unique if C_i contains only two literals. So, let us assume that C_i contains three literals. In this case, a circuit cover of $H(C_i)$ consists of exactly four circuits. Two of them are the triangles containing h_2 and h_3 and their respective opposite edges. There exist exactly two possibilities for the other two circuits (see Figure 6). Note that the circuit containing h_1 must contain either e_2 or e_3.

The triangles containing h_2 and h_3 together with the two possible circuits containing h_1 induce paths in $H(C_i)$ (thinking of $H(C_i)$ as a subgraph of M). We refer to these paths as *chains*. Similarly, there exist two chains if C_i contains only two literals. So, with each chain of $H(C_i)$ is associated a literal of the clause C_i, and for each literal of C_i there exists a corresponding chain in $H(C_i)$. In the case that v_r is identified with the free vertex h_1 there exist two candidate chains.

Now it is easy to see that if (M, p) admits a circuit cover then a circuit C of this cover must contain all arcs (t_j, s_{j+1}), $j = 1, \ldots, n$. In fact, if C enters a variable $L(v_j)$ through the arc (t_{j-1}, s_j) then it must use one of the zigzag paths and leave the variable through (t_j, s_{j+1}). Eventually, in the zigzag path the circuit could leave the variable $L(v_j)$ and enter a clause $H(C_i)$. But inside the clause the circuit is forced to use a chain and to return to the variable.

We say that a circuit C in M is *global* if it contains all arcs (t_j, s_{j+1}), $j = 1, \ldots, n$, and goes through each of the subgraphs $L(v_j)$ always using a zigzag path (eventually

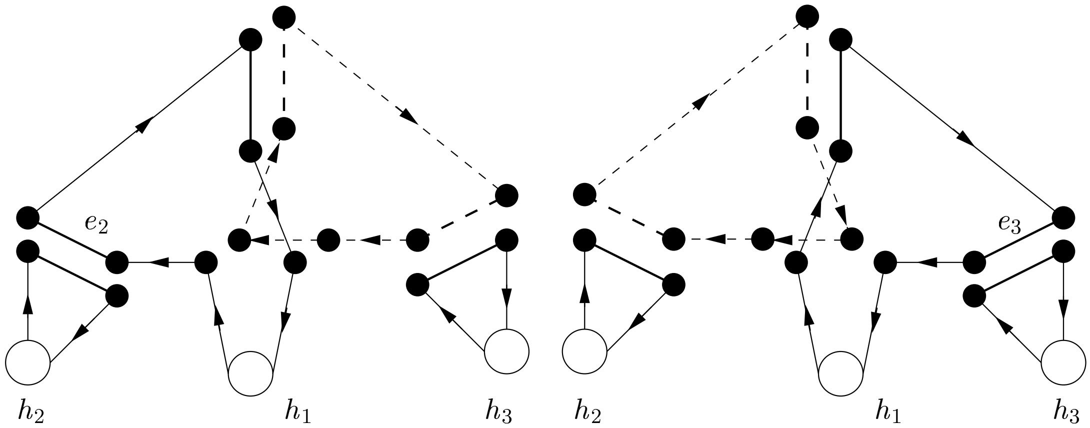

Figure 6: Possible circuits in the circuit cover of $H(C_i)$.

entering a clause $H(C_i)$, if an arc a_k was removed, using one of the corresponding chains of v_i and returning to $L(v_j)$).

Now we are able to prove that the Fractional Circuit Cover Problem and the Circuit Cover Problem for planar mixed graphs are NP-complete. We start with the proof for the latter problem. This consists of the following lemmas.

Lemma 5.1. *The graph (M, p) admits a circuit cover if and only if there exists a global circuit in M.*

Proof. As we have seen, if (M, p) admits a circuit cover then there exists a global circuit in M.

On the other hand, if M contains a global circuit C then it is easy to obtain a circuit cover of (M, p) using C and local circuits of each variable $L(v_j)$ and each clause $H(C_i)$. ∎

Lemma 5.2. *The graph M contains a global circuit if and only if the formula F is satisfiable.*

Proof. Suppose that M contains a global circuit C. Note that C cannot use three chains of $H(C_i)$ and hence, for each clause C_i there exists a literal of C_i whose corresponding chain is not used by C. Assigning true to these literals we obtain a satisfying truth assignment for F. Note that this choice is consistent because if C uses a zigzag path of a literal in $L(v_j)$ then it is forced to pass through all clauses $H(C_i)$ that contain this literal using its corresponding chain.

If F has a satisfying truth assignment then we can define a global circuit as follows. We traverse M through the "circuit" $(v_1, \ldots, v_n, v_1)$ in the adequate way in each variable $L(v_j)$: if v_j ($\overline{v}_j$) is false, choose the zigzag path that uses all arcs a_k ($\overline{a}_k$), $k = 1, \dots, 4m_j$. If this path enters a clause $H(C_i)$ we traverse a corresponding chain of v_j as follows. If v_j is not identified with the free vertex then there exists only one choice. Otherwise, C_i has three literals and one of them makes the clause true. So, we traverse the corresponding chain of v_j that contains the opposite edge of the true literal. Note that since the literal makes the clause true, the circuit C cannot enter again the clause through the corresponding variable. This defines a global circuit C. ∎

From Lemmas 5.1 and 5.2 we can conclude the following.

Theorem 5.1. *The Circuit Cover Problem for planar mixed graphs is NP-complete even with weights restricted to* 1 *and* 2. ∎

Finally, we have to verify that the Fractional Circuit Cover Problem for planar mixed graphs is NP-complete. It is sufficient to show that Lemma 5.1 remains valid if we replace "circuit cover" with "fractional circuit cover".

Lemma 5.3. *The graph* (M, p) *admits a fractional circuit cover if and only if there exists a global circuit in* M.

Proof. If M contains a global circuit, we can obtain a circuit cover as in the proof of Lemma 5.1.

On the other hand, suppose that $\lambda_1, \dots, \lambda_t$ and $C_1, \dots, C_t$ correspond to a fractional circuit cover of (M, p). First, let v be a vertex in (M, p) of degree 3. This vertex is an extreme of an edge (of weight 2 and two arcs (one entering v and other leaving v) of weight 1. Then, no circuit C_i can use both arcs incident to v. Otherwise, the edge incident to v would have a positive excess which could not be covered by other circuits. Hence, it is not hard to see that a circuit C_i containing the arc (t_n, s_1) must be a global circuit. ∎

From Lemmas 5.2 and 5.3 we have the following.

Theorem 5.2. *The Fractional Circuit Cover Problem for planar mixed graphs is NP-complete even with weights restricted to* 1 *and* 2. ∎

Finally, we note that one can prove in a similar way that the decision versions of the following problems are NP-complete for planar mixed graphs [9]: deciding whether a weighted mixed graph contains a negative circuit and finding a shortest path between two given vertices (these were known to be NP-complete for general mixed graphs [5, 3]).

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